REMARKS

This response is intended as a full and complete response to the Office Action dated June 15, 2005. In view of the amendments and the following discussion, the applicants believe that all claims are in allowable form.

I. OBJECTIONS

a) DRAWINGS

The Examiner has objected to the drawings of Figures 65-69 as not legible due to excessive saturation. A set of replacement drawings of Figures 65-69, as amended, accompanies present communication. As such, the applicants respectfully request that the objections be withdrawn.

b) CLAIMS

Claim 4 and 9

The Examiner has objected to claim 4 due to improper numbering and to claim 9 as containing limitations expressed in unclear language. In response, the Applicants have amended limitations and numbering of claim 4 and amended the recitations in claim 9 as well as claim 8 from which claim 9 depends. As such, the applicants respectfully request that the objections be withdrawn.

II. CLAIM REJECTIONS

A. 35 U.S.C. §112 Claims 1, 7-18, and 26

The Examiner rejected claims 1, 7-18, and 26 as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Specifically, the Examiner stated that claims 1, 7-18, and 26 are rejected due to insufficient antecedent basis for certain limitations. In response, the applicants have amended claims 1, 7, 8, 10, 11 and 26 accordingly. The Applicants submit that claims 1, 7-18, and 26, as they now stand, fully satisfy the requirements of 35 U.S.C. § 112. As such, the Applicants respectfully request the rejection be withdrawn.

B. 35 U.S.C. §102(b) Claims 1-6, 19-36, 38 and 44-46

Claims 1-4 and 9-10 stand rejected as being anticipated by United States Patent No. 5,663,900 issued Sep. 2, 1997 to *Bhandari et al.* (hereinafter referred to as "*BH'900*"). In response, the Applicants submit the following remarks.

The Examiner contends that *BH'900* teaches each and every limitation of the present invention including a "shared memory". The Applicants respectfully disagree.

BH'900 teaches an electronic design and verification system where a workstation 5 contains electronic design automation (EDA) system 10. The system 10 is implemented as an application program that communicates to a target board 46 ("user design" or "user circuit") via an add-on circuit card 38 and a pod (wiring assembly) 42. Interconnections between the workstation 5, the add-on circuit card 38, the pod 42, and the target board 46 are provided in a form of respective individual series links using point-to-point cables (FIG. 1; col. 2, lines 28-44). The system 10 includes a simulator for simulating or emulating a functional specification of a particular prototype. The component models used by the simulation are stored in memory or a database (col. 3, lines 36-43). *BH'900* does not teach a shared memory that stores information for both a software model and a hardware model.

In contrast to the teachings of *BH'900,* the applicant's claim 1 specifically recites "shared memory for holding a first information of a software model and a second information of the hardware model". *BH'900* simply does not contain a memory that is shared by a software model and a hardware model. The other independent claims 19, 24, 30, 33, 38, 44 contain a similar recitation to a shared memory.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Therefore, Applicants contend that claims 1, 19, 24, 30, 33, 38, and 44 are patentable over *BH'900* and, as such, fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder.

Furthermore, claims 2-6, 20-23, 25-29, 31-36, and 45-46 depend, either directly or indirectly, from claims 1, 19, 24 30, 33, 38, and 44 and recite additional features therefor. Since *BH'900* does not teach Applicants' invention as recited in claims 1, 19, 30, 33, 38, and 44, dependent claims 2-6, 20-23, 27-28, 34-36, and 45

are also patentable over *BH'900*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

C. 35 U.S.C. §103(a) Claims 7 and 10

Claims 7 and 10 stand rejected as being unpatentable over *BH'900* in view of an article "Q-Modules: Internally Clocked Delay-Insensitive Modules" by Rosenberger et al. (IEEE Transactions on Computers, vol. 37, No. 9, Sep. 1988, pp. 1005-1018, hereinafter referred to as "*RO'1988*"). The applicants respectfully traverse the rejection.

The Examiner contends that *BH'900* teaches all the limitations of claims 7 and 10 except the timing logic. The Examiner cites *RO'1988* as teaching timing logic. The Examiner concludes that a combination of *BH'900* and *RO'1988* teach the subject matter of claims 7 and 10. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in claim 1 from which claims 7 and 10 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *RO'1988* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 7 and 10) that depend from claim 1 are not taught or suggested by the cited references.

Thus, the applicants submit that claims 7 and 10 are patentable over *BH'900* in view of *RO'1988*. Accordingly, the applicants respectfully request the rejection be withdrawn.

D. 35 U.S.C. §103(a) Claims 8-9 and 11-18

Claims 8-9 and 11-18 stand rejected as being unpatentable over *BH'900* in view of *RO'1988* and further view of an article "High Speed External Asynchronous/Internally clocked Systems" by VanScheik et al. (IEEE Transactions on Computers, vol. 46, No. 7, Jul. 1997, pp. 824-829, hereinafter referred to as "*VA'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 8-9 and 11-18 except the timing logic having a first logic, second logic and third logic.

The Examiner cites *RO'1988* as teaching timing logic, but the Examiner concedes that RO'1988 does not teach the first, second and third logic. As such, the Examiner cites *VA '1997* as teaching first logic, second logic and third logic. The Examiner concludes that a combination of *BH'900, RO'1988* and *VA'1997* teach the subject matter of claims 8-9 and 11-18. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in claim 1 from which claims 8-9 and 11-18 depend. *RO'1988* teaches Q-modules without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model and VA'1997 teaches delay insensitive logic modules. Since neither the *BH'900, RO'1988* nor *VA'1997* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 1) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 8-9 and 11-18) that depend from claim 1 are not taught or suggested by the cited references.

Furthermore, claims 8-9 and 11-18 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since the combination of *BH'900*, *RO'1988* and *VA'1997* does not teach or suggest the applicants' invention as recited in claim 1, dependent claims 8-9 and 11-18 are also not obvious and are allowable.

Thus, the applicants submit that claims 8-9 and 11-18 are patentable over *BH'900* in view of *RO'1988* and *VA'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

E. 35 U.S.C. §103(a) Claim 37

Claim 37 stands rejected as being unpatentable over *BH'900* in view of United States Patent No. 5,661,662 issued Sep. 2, 1997 to *Butts et al.* (hereinafter referred to as "*BU'662*").

The Examiner contends that *BH'900* in view of *BU'662* teaches all the limitations of claim 37 except "a plurality of field programmable logic devices couple together separable by at most two interconnections." The Examiner cites *BU'662* as teaching such programmable logic devices. The Examiner concludes that a combination of *BH'900* and *BU'662* teach the subject matter of claim 37. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in

claim 33 from which claim 37 depends. *BU'662* teaches interconnected FPGAs without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *BU'662* contain a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claim (claim 37) that depends from claim 33 are not taught or suggested by the cited references.

Therefore, the applicants submit that claim 37 is patentable over *BH'900* in view of *BU'662*. Accordingly, the applicants respectfully request the rejection be withdrawn.

F. 35 U.S.C. §103(a) Claim 39-43 and 47-50

Claims 39-43 and 47-50 stand rejected as being unpatentable over *BH'900* in view of an article "A Heterogeneous Environment for Hardware/Software Cosimulation" by Bishop et al. (IEEE Transactions on Computers, 1997, pp. 14-22, hereinafter referred to as "*BI'1997*").

The Examiner contends that *BH'900* teaches all the limitations of claims 38 and 44, except a plurality of field programmable devices as recited in the dependent claims. The Examiner cites *BI'1997* as teaching such devices as well as other limitations of claims 39-43 and 47-50. The Examiner concludes that a combination of *BH'900* and *BI'1997* teach the subject matter of claims 39-43 and 47-50. The applicants respectfully disagree.

As discussed above, *BH'900* does not teach a shared memory as recited in independent claims 38 and 44 from which claims 39-43 and 47-50 depend. *BI'1997* teaches hardware/software co-simulation without any teaching or suggestion of using shared memory for storing information from both a hardware model and a software model. Since neither the *BH'900* nor *BI'1997* teach a shared memory, no combination of these references can teach a shared memory. Consequently, an element of the base claim (claim 33) is not taught or suggested by the references taken singly or in combination. Therefore, the dependent claims (claims 39-43 and 47-50) that depend from claims 38 and 44 are not taught or suggested by the cited references.

Therefore, the applicants submit that claims 39-43 and 47-50 are patentable

over *BH'900* in view of *BI'1997*. Accordingly, the applicants respectfully request the rejection be withdrawn.

CONCLUSION

Thus, the applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Raymond R. Moser, Jr. at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

9-15-05

Respectfully submitted,

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IN THE DRAWINGS

The attached sheets of drawings include changes to FIGS. 65-69. In the amended drawings, excessive saturation has been removed from the FIGS. 65-69. The attached sheets replace the original sheets including FIGS. 65-69.